This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (original): A circuit configuration, comprising:

a ferroelectric memory component having a plurality of ferroelectric memory cells, bit lines and sense amplifiers connected to said bit lines;

a test circuit including a plurality of analog amplifiers each connected, on an input side thereof, to an associated one of said bit lines;

said test circuit being integrated in said ferroelectric memory component and having a test mode;

said sense amplifiers being in a state selected from the group consisting of a non-activated state and a disconnected state during the test mode; and

said test circuit, when in the test mode, outputting, via said analog amplifiers, analog signals from said ferroelectric memory cells and present on said bit lines connected to said ferroelectric memory cells to a point outside said

ferroelectric memory component for an external evaluation of the analog signals.

Claim 2 (original): The circuit configuration according to claim 1, wherein:

said ferroelectric memory component includes a test pad; and

said analog amplifiers have respective outputs connected to said test pad.

Claim 3 (original): The circuit configuration according to claim 1, wherein:

said ferroelectric memory component includes a test pad; and

said test circuit has an output connected to said test pad.

Claim 4 (original): The circuit configuration according to claim 1, wherein:

said ferroelectric memory component includes a test pad;

said test circuit has an output; and

a switching device is provided at said output of said test circuit, said switching device switches analog output signals to said test pad.

Claim 5 (original): The circuit configuration according to claim 1, wherein:

said ferroelectric memory component includes a test pad;

said analog amplifiers have respective outputs; and

a switching device is provided at said outputs of said analog amplifiers, said switching device switches analog output signals to said test pad.

Claim 6 (original): The circuit configuration according to claim 1, wherein:

said ferroelectric memory component includes an output terminal;

said test circuit has an output; and

a switching device is provided at said output of said test circuit, said switching device switches analog output signals

to said output terminal of said ferroelectric memory component.

Claim 7 (original): The circuit configuration according to claim 1, wherein:

said ferroelectric memory component includes an output terminal;

said analog amplifiers have respective outputs; and

a switching device is provided at said outputs of said analog amplifiers, said switching device switches analog output signals to said output terminal of said ferroelectric memory component.

Claim 8 (original): The circuit configuration according claim 1, wherein:

said ferroelectric memory component includes an output terminal; and

at least one of said test circuit and said analog amplifiers are configured such that analog bit line signals are output with a given resolution and without influencing bit line potentials at said output terminal.

Claim 9 (original): The circuit configuration according claim 1, wherein:

said ferroelectric memory component includes a test pad; and

at least one of said test circuit and said analog amplifiers are configured such that analog bit line signals are output with a given resolution and without influencing bit line potentials at said test pad.

Claim 10 (original): The circuit configuration according to claim 1, wherein said test circuit and said ferroelectric memory component are configured to be fabricated simultaneously in accordance with a CMOS process.

Claim 11 (original): A circuit configuration, comprising:

a ferroelectric memory component having a plurality of ferroelectric memory cells, bit lines and sense amplifiers connected to said bit lines;

a test circuit including an analog amplifier provided for said bit lines, said analog amplifier having an input;

a switching device connected to said input of said analog amplifier and configured to switch analog signals from said bit lines successively to said input of said analog amplifier;

said test circuit being integrated in said ferroelectric memory component and having a test mode;

said sense amplifiers being in a state selected from the group consisting of a non-activated state and a disconnected state during the test mode; and

said test circuit, when in the test mode, outputting, via said analog amplifier, analog signals from said ferroelectric memory cells and present on said bit lines connected to said ferroelectric memory cells to a point outside said ferroelectric memory component for an external evaluation of the analog signals.

Claim 12 (currently amended): The circuit configuration according to claim ~~10~~ 11, wherein:

said ferroelectric memory component includes a test pad; and

said analog amplifier has an output connected to said test pad.

Claim 13 (currently amended): The circuit configuration according to claim ~~10~~ 11, wherein:

said ferroelectric memory component includes a test pad; and

said test circuit has an output connected to said test pad.

Claim 14 (currently amended): The circuit configuration according to claim ~~10~~ 11, wherein:

said ferroelectric memory component includes a test pad;

said test circuit has an output; and

a further switching device is provided at said output of said test circuit, said further switching device switches analog output signals to said test pad.

Claim 15 (currently amended): The circuit configuration according to claim ~~10~~ 11, wherein:

said ferroelectric memory component includes a test pad;

said analog amplifier has an output; and

a further switching device is provided at said output of said analog amplifier, said further switching device switches analog output signals to said test pad.

Claim 16 (currently amended): The circuit configuration according to claim ~~10~~ 11, wherein:

said ferroelectric memory component includes an output terminal;

said test circuit has an output; and

a further switching device is provided at said output of said test circuit, said further switching device switches analog output signals to said output terminal of said ferroelectric memory component.

Claim 17 (currently amended): The circuit configuration according to claim ~~10~~ 11, wherein:

said ferroelectric memory component includes an output terminal;

said analog amplifier has an output; and

a further switching device is provided at said output of said analog amplifier, said further switching device switches analog output signals to said output terminal of said ferroelectric memory component.

Claim 18 (currently amended): The circuit configuration according claim ~~10~~ 11, wherein:

said ferroelectric memory component includes an output terminal; and

at least one of said test circuit and said analog amplifier are configured such that analog bit line signals are output with a given resolution and without influencing bit line potentials at said output terminal.

Claim 19 (currently amended): The circuit configuration according claim ~~10~~ 11, wherein:

said ferroelectric memory component includes a test pad; and

at least one of said test circuit and said analog amplifier are configured such that analog bit line signals are output with a given resolution and without influencing bit line potentials at said test pad.

Claim 20 (currently amended): The circuit configuration according to claim ~~10~~ 11, wherein said test circuit and said ferroelectric memory component are configured to be fabricated simultaneously in accordance with a CMOS process.